CLAIMS

What is claimed is:

1. A method for performing data transfers within a computer system, the method comprising the steps of:

causing a controller to perform the steps of

transmitting control information on a bus, the control information specifying a data transfer operation and a first location of data to be transferred;

after transmitting the control information on the bus, performing the steps of

determining a desired amount of data to be transferred in the data transfer operation;

transmitting over the bus additional locations of data if the desired amount of data is greater than a predetermined amount of data;

transmitting over the bus a terminate indication at a time that is based on the desired amount of data to be transferred;

causing a memory device to perform the steps of

reading the control information on the bus;

performing the specified data transfer operation on data stored at the first location;

performing the specified data transfer operation on data stored at the additional locations when the desired amount of data is greater than the amount of data associated with the first location;

continuing to perform the specified data transfer operation until detecting the terminate indication on the bus;

ceasing to perform the data transfer operation at a time that is based on the time at which the terminate indication is detected.

2. The method of Claim 1 further comprising the steps of:

causing the controller to transmit a strobe signal on the bus after transmitting the control information; and

causing the memory device to begin performing the specified data transfer operation at a time that is based upon when the memory device detects the strobe signal on the bus.

3. The method of Claim 2 further comprising the steps of:

causing the controller to select an interleave pattern based on the specified data transfer operation and requests received for one or more data transfer operations other than the specified data transfer operation; and

causing the controller to transmit control information over the bus for at least one of the one or more data transfer operations after transmitting the control information for the specified data transfer operation and prior to transmitting the strobe signal.

4. The method of Claim 1 further comprising the steps of:

during the transfer operation, causing the controller to determine whether the memory device is to perform a precharge operation after the memory device performs the data transfer operation;

at or about the end of the data transfer operation, causing the controller to communicate to the memory device whether the memory device is to perform a precharge operation after the memory device performs the data transfer operation.

5. The method of Claim 4 further wherein the step of causing the controller to communicate to the memory device whether the memory device is to perform a precharge operation after the memory device performs the data transfer operation includes the steps of:

establishing a correlation between a plurality of clock cycles and a plurality of precharge options;

selecting a precharge option from the plurality of precharge options; and

causing the controller to transmit the termination indication during a clock cycle that corresponds to the selected precharge option.

6. A memory device for storing data and performing data transfer operations, the memory device comprising:

control circuitry coupled to a bus; and

memory for storing data;

wherein the control circuitry is configured to read control information carried on the bus;

wherein the control information includes data that specifies a data transfer operation and a first address;

wherein the memory device is configured to perform the specified data transfer operation on data stored in the memory beginning at the first address;

wherein the memory device is configured to perform the specified data transfer operation on data stored beginning at additional locations specified in address information carried over the bus until detecting a terminate indication on the bus; and

wherein the memory device ceases to perform the data transfer operation at a time that is based on the time at which the terminate indication is detected.

7. The memory device of Claim 6 further configured to detect a strobe signal on the bus, and to begin performing the specified data transfer operation at a time based on the time at which the strobe signal is detected.

8. The memory device of Claim 6 further configured to read address information carried on one or more lines of the bus while performing the specified data transfer operation using one or more other lines of the bus, wherein the address information specifies where data involved in the specified data transfer operation is located.

9. The memory device of Claim 7 wherein the control information specifies a location of a first set of data, the memory device being configured to retrieve the first set of data from the location prior to detecting the strobe signal.

10. The memory device of Claim 9 wherein:

the memory device is further configured to read address information from one or more lines of the bus,

the address information specifies locations for one or more additional sets of data to be transmitted in the data transfer operation,

the memory device retrieves the one or more additional sets of data upon reading the address information, and

the memory device transmits the one or more additional sets of data after transmitting the first set of data.

11. A method, for use in a memory controller, for maximizing usage of a bus that connects the memory controller to one or more memory devices, the method comprising the steps of:

selecting an interleave pattern based on requests received for a plurality of data transfer operations; and

for each data transfer operation of the plurality of data transfer operations transmitting control information over the bus, wherein the control information specifies the data transfer operation;

determining how much time must elapse between transmission of the control information and the start of the data transfer operation to provide the interleave pattern; and

transmitting a start indicator over the bus that specifies when the data transfer operation is to begin.

12. The method of Claim 11 wherein the step of transmitting a start indicator is performed by transmitting a delay value in the control information, the delay value indicating when the data transfer operation is to begin relative to the time at which the control information is transmitted over the bus.

13. The method of Claim 11 wherein the step of transmitting a start indicator is performed by transmitting a strobe signal a selected number of clock cycles after transmitting the control information, wherein the number of clock cycles is determined based on how much time must elapse between transmission of the control information and the start of the data transfer operation to provide the interleave pattern.

14. A method for reducing the number of lines required to transmit control information to one or more memory devices, the method comprising the steps of:

transmitting a request packet that specifies a data transfer operation over a channel to which the one or more memory devices are connected, wherein the request packet includes a value that indicates how to

identify a strobe signal associated with the data transfer operation that will appear on a particular control line of the channel;

transmitting zero or more control signals with signal characteristics identical to the strobe signal on the particular control line after transmitting the request packet and prior to transmitting the strobe signal; and

transmitting the strobe signal on the particular control line.

15. The method of Claim 14 wherein the value indicates how many signals that are identical to the strobe signal will appear on the particular control line prior to the strobe signal.

16. The method of Claim 14 wherein the data transfer operation is one of a plurality of data transfer operations to be performed over the channel, the method further comprising the step of dynamically determining an interleave pattern for the plurality of data transfer operations, wherein the amount of time between the transmission of the request packet and the transmission of the strobe signal varies based on the interleave pattern.

17. The method of Claim 14 further comprising the steps of

causing the one or more memory devices to enter a powered down mode in which the one or more memory devices do not monitor the channel; and

transmitting a wakeup signal over the particular control line prior to transmitting the request packet, the wakeup signal causing the memory device of the one or more memory devices that is required to service the data transfer operation to exit the power down mode and to begin monitoring the channel.

18. A method, for use by a memory controller coupled to a memory device over a bus, for deferring precharge decisions, the method comprising the steps of:

transmitting a request packet to the memory device over a first number of lines of the bus, wherein the request packet specifies a data transfer operation;

receiving requests for additional data transfer operations while the memory device is performing the data transfer operation;

determining, based on the requests received for the additional transfer transactions, whether a precharge operation should be initiated after the data transfer operation;

transmitting to the memory device over a second number of lines of the bus, at or about the end of the data transfer operation, a control signal that indicates whether a precharge operation should be initiated after the data transfer operation, wherein the second number of lines is less than the first number of lines.

19. The method of Claim 18 wherein the step of transmitting the control signal is performed by transmitting a termination signal to the memory device, the memory device terminating the data transfer operation at a time that is based on when the memory device receives the termination signal.

20. The method of Claim 19 wherein:

the memory device is configured to terminate the data transfer operation after a particular data packet is transmitted if the memory device detects the termination signal on any one of a plurality of clock cycles;

the memory controller indicates that a precharge operation is to be performed by transmitting the termination signal on a particular clock cycle of the plurality of clock cycles;

the memory controller indicates that a precharge operation is not to be performed by transmitting the termination signal on a different clock cycle of the plurality of clock cycles; and

the memory device initiates a precharge operation based the clock cycle on which the termination signal is detected by the memory device.

21. The method of Claim 19 wherein:

the memory device contains a plurality of banks;

the memory device terminates the data transfer operation after a particular data packet is transmitted if the memory device detects the termination signal on any one of a plurality of clock cycles;

the method further includes the step of establishing a correspondence between the plurality of clock cycles and the plurality of banks;

the memory controller indicates a bank within the memory device on which a precharge operation is to be performed by transmitting the termination signal on the clock cycle of the plurality of clock cycles that corresponds to the bank; and

the memory device initiates a precharge operation on the bank that corresponds to the clock cycle on which the memory device detects the termination signal.

22. A method for performing a data transfer operation, the method comprising the steps of:

causing a controller to perform the steps of

constructing an operation code for the data transfer operation, the operation code including a plurality of bits that correspond to a plurality of control lines within a memory device; and

transmitting the operation code to the memory device over a bus;

causing the memory device to perform the steps of

receiving the operation code over the bus;

for each control line of the plurality of control lines, applying a signal to the control line based on the value of the bit that corresponds to the control line in the operation code; and

performing the data transfer operation specified in the operation code.

23. The method of Claim 22 wherein:
one of the control lines is a write control line;
the plurality of bits includes a bit that corresponds to the write control line;
the method further comprises the steps of:
the controller setting the bit that corresponds to the write control line based on whether the data transfer operation is a write operation or a read operation; and
the memory device applying a signal to the write control line based on whether the bit that corresponds to the write control line is set.

24. The method of Claim 22 wherein:
the memory device includes a plurality of registers;
one of the control lines is a register control line;
the plurality of bits includes a bit that corresponds to the register control line;
the method further comprises the steps of:
the controller setting the bit that corresponds to the register control line based on whether the data transfer operation is a register operation; and
the memory device applying a signal to the register control line based on whether the bit that corresponds to the register control line is set.

25. The method of Claim 22 wherein:

the step of receiving the operation code over the bus includes receiving each of the plurality of bits at different pins of the memory device;

the method further comprises the steps of

routing each of the bits from the pin on which it was received to a decoder associated with the control line to which the bit corresponds;

causing the decoder associated with each control line to apply a signal to the control line based on the bit that corresponds to the control line and state information maintained in the decoder.

26. A method for use by a memory device to determine whether to process a request packet, the method comprising the steps of:

receiving the request packet over a bus, the request packet including an operation code that specifies a data transfer operation and an address;

comparing the address in the request packet to an address associated with the memory device; and

processing the request packet if either

the address in the request packet matches the address associated with the memory device, or

a particular bit in the operation code has a particular state.

27. A method for performing data transfer operations, the method comprising the steps of:

causing a controller to perform the steps of:

receiving a request for a data transfer operation;

determining a memory device that will be involved in the data transfer operation;

determining whether the memory device should perform any internal memory core operations before or after performing the data transfer operation;

transmitting over a bus control information that includes a first set of bits that specify the data transfer operation and a second set of bits that specify zero or more internal memory core operations to be performed by the memory device;

causing the memory device to perform the steps of:

receiving the control information over the bus;

performing the data transfer operation specified in the first set of bits; and

performing the internal memory core operations specified in the second set of bits.

28. The method of Claim 27 wherein the second set of bits specifies a sequence to the data transfer operation and the internal memory core operations, the

memory device performing the data transfer operation and the internal memory core operations in the sequence specified by the second set of bits.

29. The method of Claim 27 wherein:
the controller maintains a record of a current state of the memory device; and
the step of determining whether the memory device should perform any internal memory core operations is performed by the controller based on the current state of the memory device.

30. The method of Claim 29 wherein:
the controller maintains a record of an address of data that is currently stored in sense amplifiers in the memory device; and
the controller performs the step of determining whether the memory device should perform any internal memory core operations based on the address of data that is currently stored in sense amplifiers in the memory device and an address of the data involved in the data transfer operation.

31. A memory device for storing digital data, the memory device including:
a power supply line;
a plurality of banks coupled to the power supply line, each bank of the plurality of banks drawing current from the power supply line when a core operation is performed on the bank;

control circuitry coupled to the plurality of banks and to an external bus, the control circuitry receiving requests for data transfer operations over the external bus;

the control circuitry being configured to detect when performance of any of the data transfer operations would result in core operations being concurrently performed on two or more of the plurality of banks; and

the control circuitry being configured to perform each of the data transfer operations only if performance of the data transfer operation would not result in core operations being concurrently performed on two or more of the plurality of banks.

32. The memory device of Claim 31 further comprising a queue that corresponds to all banks on the power supply line, the control circuitry placing data transfer operations that require performance of core operations on any of the plurality of banks into the queue, the control circuitry sequentially servicing the queue to prevent core operations from being concurrently performed on two or more of the plurality of banks.

33. The memory device of Claim 31 wherein the control circuitry is configured to ignore each data transfer operation whose execution would result in core operations being concurrently performed on two or more of the plurality of banks.

34. The memory device of Claim 31 further comprising a queue, the control circuitry placing data transfer operations that require performance of core operations on any banks in the memory device into the queue, the control circuitry sequentially servicing the queue to prevent core operations from being concurrently performed on two or more banks within the memory device.

35. A memory device for use in a computer system that includes a controller coupled to a channel, the memory device comprising:

an input circuit coupled to the channel, the input circuit being configured to receive control information from the controller over the channel, the control information specifying data transfer operations, wherein the data transfer operations include some data transfer operations that require core operations must be performed for the memory device to perform the data transfer operations;

a plurality of memory banks;

a power supply line coupled to the plurality of memory banks, the power supply line for carrying current to the plurality of memory banks to supply current required to perform the core operations, the power supply line being configured to reliably supply current for no more than one core operation at a time;

control circuitry coupled to the input circuit, the control circuitry being configured to cause the memory device to perform the data transfer operations specified in the control information without regard to

whether performance of the transfer transactions would cause more than one core operation to be concurrently performed on the plurality of memory banks, the controller controlling transmission of the control information to prevent more than one core operation from being concurrently performed on the plurality of memory banks.

36. A method for performing data transfers within a computer system, the method comprising the steps of:

causing a controller to perform the steps of

transmitting control information on a bus, the control information specifying a data transfer operation and a first location of data to be transferred;

determining a delay interval;

transmitting a control signal over the bus after the delay interval has elapsed from when the step of transmitting the control information on the bus was performed;

causing a memory device to perform the steps of

reading the control information on the bus;

detecting the control signal on the bus;

performing the specified data transfer operation on data stored at the first location at a time based on when the control signal was detected on the bus.

37. The method of Claim 36 further comprising the step of causing the controller to change the delay interval for successive data transfer operations.

38. The method of Claim 36 further comprising the step of causing the controller to determine a desired interleave, wherein the controller performs the step of determining a delay interval based on the desired interleave.

39. The method of Claim 36 further comprising the steps of:

causing the controller to transmit a terminate signal over the bus; and

causing the memory device to continue to perform the data transfer operation until detecting the terminate signal on the bus.

40. A memory controller configured to maximize usage of a bus that connects the memory controller to one or more memory devices, the memory controller comprising:

a control unit configured to select an interleave pattern based on requests received for a plurality of data transfer operations; and

an output unit coupled to the control unit and to the bus;

the control unit being further configured to perform the following steps for each data transfer operation of the plurality of data transfer operations:

transmitting control information through the output unit to the bus, wherein the control information specifies the data transfer operation;

determining how much time must elapse between transmission of the control information and the start of the data transfer operation to provide the interleave pattern; and

transmitting a start indicator through the output unit to the bus, wherein the start indicator specifies when the data transfer operation is to begin.

41. The memory controller of Claim 40 wherein the step of transmitting a start indicator is performed by transmitting a delay value in the control information, the delay value indicating when the data transfer operation is to begin relative to the time at which the control information is transmitted over the bus.

42. The memory controller of Claim 40 wherein the step of transmitting a start indicator is performed by transmitting a strobe signal a selected number of clock cycles after transmitting the control information, wherein the number of clock cycles is determined based on how much time must elapse between transmission of the control information and the start of the data transfer operation to provide the interleave pattern.

add 41